28.3 A 10Gb/s CMOS AGC Amplifier with 35dB Dynamic Range for 10Gb Ethernet

Chih-Fan Liao, Shen-Iuan Liu

National Taiwan University, Taipei, Taiwan

Multimode fibers are widely used in today's LAN links such as 10Gigabit Ethernet. To compensate modal dispersion, which limits the transmission distance, an equalizer in the receiver is mandatory. However, there are two issues to consider if an FIR filter is used. First, to perform accurate dispersion compensation, a large number of taps is often required, which introduces significant noise at the output and degrades the receiver sensitivity because of the limited gain of the transimpedance amplifier preceding the equalizer. Second, since an FIR filter linearly combines input signals with different delays, any nonlinear distortion caused by overdriving the taps of the equalizer must be avoided. The noise and linearity issues are much relaxed if an automatic gain control (AGC) amplifier precedes the equalizer, as shown in Fig. 28.3.1. In this paper, a 10Gb/s AGC amplifier with 35dB DR is implemented in 0.18μm CMOS technology. To the author's knowledge, this is the first CMOS AGC amplifier operating at 10Gb/s.

Figure 28.3.1 depicts the architecture of the AGC amplifier. It consists of a variable gain amplifier (VGA), a two-stage post amplifier, and some control circuits, which include an exponential voltage generator, a peak detector, and an integrator. The exponential voltage generator produces linear-in-dB control of the VGA gain. The post amplifier provides additional gain to increase the sensitivity. The peak detector and integrator serve as the AGC loop according to the reference voltage, V_{REF}. An offset-cancellation loop is built to eliminate the dc offset due to device mismatches. An output buffer is also included for driving a 50Ω off-chip load.

Conventionally, pseudo-exponential functions [1] and successive approximation [2] are used to realize linear-in-dB VGAs in CMOS technology. The pseudo-exponential function [1] achieves a 42dB-linear gain range per stage but has two problems for a 10Gb/s VGA. First, the circuit needs an active common-mode feedback, which contributes large parasitic capacitance at the output. Second, the square-law relationship between I_D and V_{GS} no longer holds when velocity saturation occurs in a short-channel transistor. This degrades the gain range as well as tuning linearity. The successive approximation method [2] requires multiple transistors in parallel to achieve a large dB-linear range. This increases capacitance at the output and lowers the speed. When combined with the inductive peaking technique, the bandwidth and group delay vary considerably under different gain modes, causing severe ISI. To obtain a wide linear-in-dB tuning range and a constant bandwidth, we adopt a folded Gilbert cell in combination with an exponential voltage generator, which is depicted in Fig. 28.3.2. The folded transistors ($M_{5,6}$) can sustain large V_{GS} to achieve the required linearity between the VGA gain and the control voltage ($V_{C+} - V_{C-}$) without requiring degeneration. The low speed of the AGC loop also makes it possible to use parasitic vertical BJTs to generate the exponential function. In this triple-well process, we adopt vertical NPN transistors to obtain larger β and higher current driving capability. The exponential current passes through two resistors, R, making ($V_{C+} - V_{C-}$) vary linearly in dB. Since V_{C+} will always be greater than V_{C-}, one of the two differential pairs ($M_{1,2}$) always possesses a gain higher than the other ($M_{3,4}$). This ensures the polarity of the output and eliminates the additional current source required in [3]. This VGA achieves a linear-in-dB controlled range larger than 50dB per stage, which is difficult to achieve using a pseudo-exponential function in short-channel CMOS.

The post amplifier is composed of two gain stages. Each stage is realized as a modified Cherry-Hooper amplifier, which is depicted in Fig. 28.3.3. Conventional Cherry-Hooper amplifiers suffer from a limited bandwidth due to the drop of loop gain at high frequency. In this design, we adopt capacitive peaking to boost G_m and shunt-series inductive peaking [4] to mitigate the effect of the parasitic capacitance. The pole at node X can be partially compensated by the zero introduced by the capacitive peaking stage ($M_{5,6}$ and C_P), while the pole at node Y can be ameliorated using inductors L_1 and L_2. The inductors are realized as 3D miniature architectures [5] to achieve higher self-resonant frequenices f_{SR} and smaller area. By these combined techniques, the post amplifier achieves a gain of 15dB and a bandwidth of 10GHz while drawing 19mA of bias current. This bandwidth is 3 times larger than is obtained by cascading conventional Cherry-Hooper amplifiers, but the gain and power are the same.

The peak detector is implemented as a source-coupled pair followed by low-pass filtering. Because of the high tuning sensitivity of the exponential voltage generator, the gain of the peak detector can be lower than it would otherwise need to be. This allows the transistors to be smaller and saves power. The integrator has a unity-gain frequency of 72kHz with a 1nF external capacitor. The finite base current of the BJTs would lower the effective gain of the integrator, but is provided by the current source M_C in Fig. 28.3.2.

The AGC amplifier is implemented in 0.18μm CMOS technology and the performance was measured by probing the die, while the dc-bias connections were bonded to the PCB. Fig. 28.3.4 shows the die micrograph. The area is 1.5×0.88mm^2 including pads.

Fig. 28.3.5 shows the measured VGA gain versus control voltage with a 400MHz sine wave input. A resistive divider is built off-chip to reduce the tuning sensitivity under open-loop operation. The VGA shows a linear-in-dB control range of 58dB; from –37 to 21dB. A linearity error less than ±1dB is achieved over a 45dB gain range.

Fig. 28.3.6 depicts the measured BER versus input swing and differential output eye diagrams at 10Gb/s with 2^7-1 PRBS data. For input swings from 18mV$_{pp}$ to 1V$_{pp}$, the differential output is 430mV$_{pp}$ within +0.4 to about –0.8dB variation (394 to 450mV$_{pp}$). The measured dynamic range is 35dB with a BER less than 10^{-12}.

Fig. 28.3.7 summarizes the measured performance. The 10Gb/s AGC amplifier consumes 54mW of power from a 1.8V supply.

Acknowledgements:
The authors would like to thank MediaTek Inc., National Science Council, and National Chip Implementation Center for support of this work and chip implementation.

References:

[1] Q. H. Duong, L. Quan and S. G. Lee, "An All CMOS 84dB-Linear Low-Power Variable Gain Amplifier," *IEEE Symp. VLSI Ciruits*, pp. 114–117, 2005.

[2] Y. S. Youn et al., "A CMOS IF Transceiver with 90dB Linear Control VGA for IMT-2000 Application," *IEEE Symp. VLSI Ciruits*, pp. 131–134, 2003.

[3] C. H. Wu, C. S. Liu and S. I. Liu, "A 2GHz CMOS Variable-Gain Amplifier with 50dB Linear-in-Magnitude Controlled Gain Range for 10GBase-LX4 Ethernet," *ISSCC Dig. Tech. Papers*, pp. 484–485, Feb., 2004.

[4] T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, New York, 1998.

[5] C. C. Tang, C. H. Wu and S. I. Liu, "Miniature 3-D Inductors in Standard CMOS Process," *IEEE J. Solid-State Circuits*, vol. 37, pp. 471–480, April, 2002.

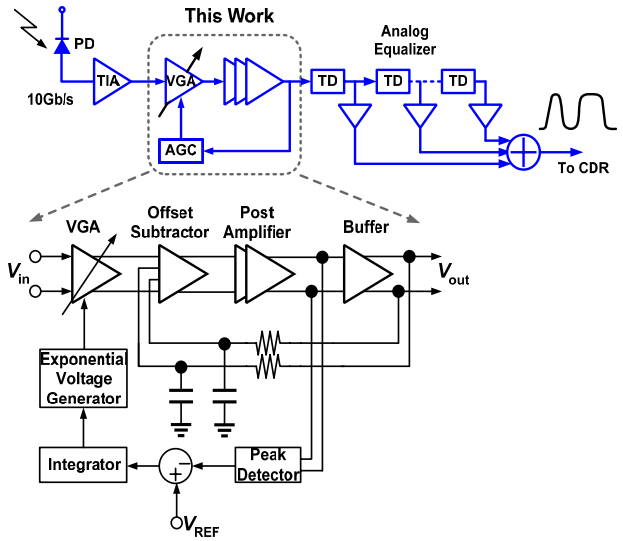

Figure 28.3.1: Architecture of the AGC amplifier for 10Gigabit ethernet.

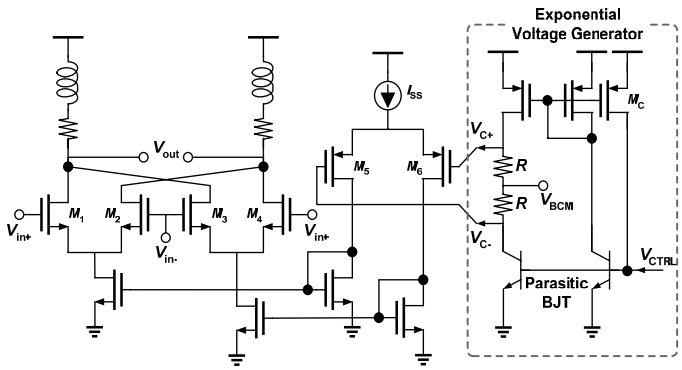

Figure 28.3.2: The proposed CMOS linear-in-dB VGA.

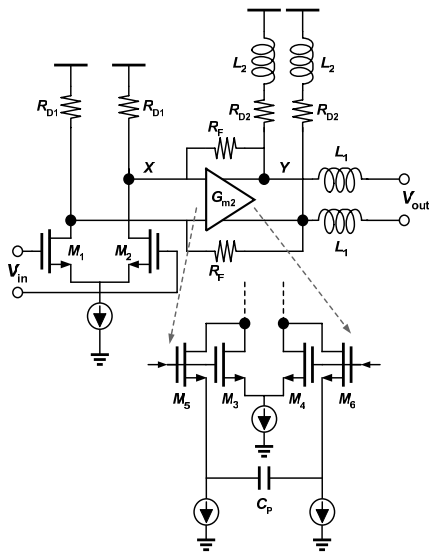

Figure 28.3.3: One of the gain stages in the post amplifier.

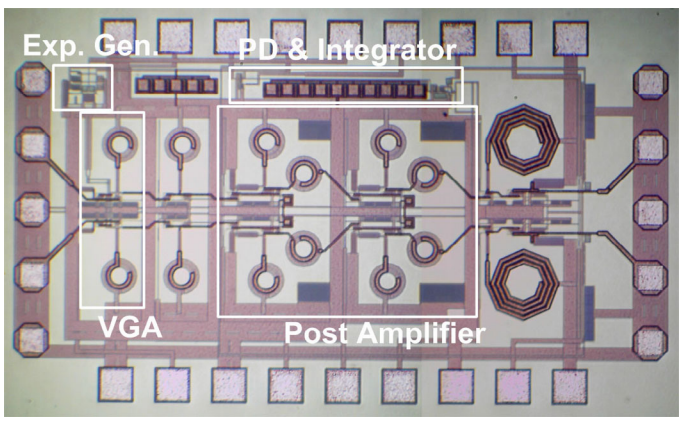

Figure 28.3.4: Die micrograph of the 10Gb/s AGC amplifier.

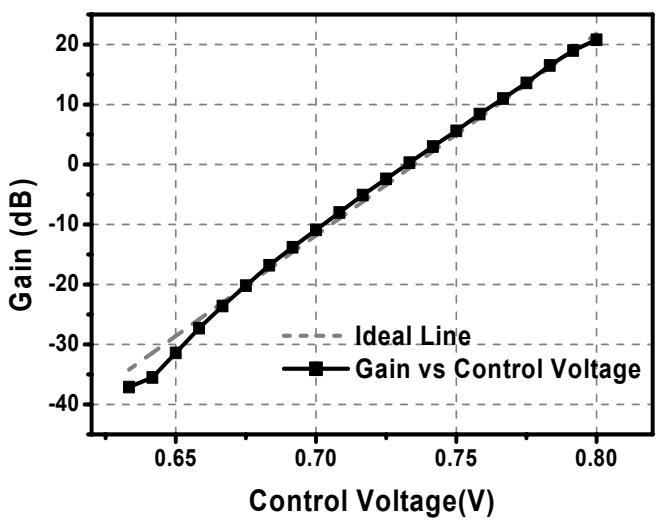

Figure 28.3.5: Measured open-loop VGA gain versus control voltage.

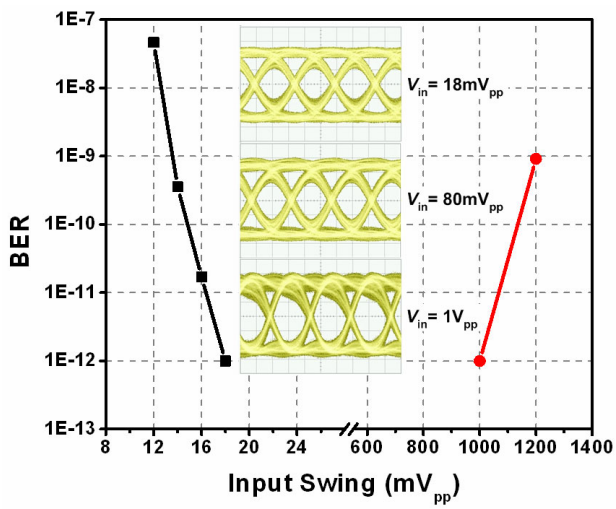

Figure 28.3.6: Measured BER versus input swing and differential output eye diagrams at 10Gb/s with 27-1PRBS data for input swings of 18mV_{pp}, 80mV_{pp}, and 1V_{pp}, respectively. (horizontal scale: 40ps/div, vertical scale: 75mV/div).

Continued on Page 670

Technology	0.18μm CMOS
Data Rate	10Gb/s
VGA Tuning Range	58dB (–37dB ~ 21dB*)
Dynamic Range @BER<10^{-12}	35dB ($18mV_{pp}$ – $1V_{pp}$)
Peak-to-Peak Jitter	< 25ps
Harmonic Distortion	HD3 < –29dBc
Input Referred Noise	$378\mu V_{rms}$
Power Dissipation	54mW
Supply Voltage	1.8V
Area	1.5mm x 0.88mm

*: with a linearity error less than ±1dB over 45dB

Figure 28.3.7 Measured performance summary.

